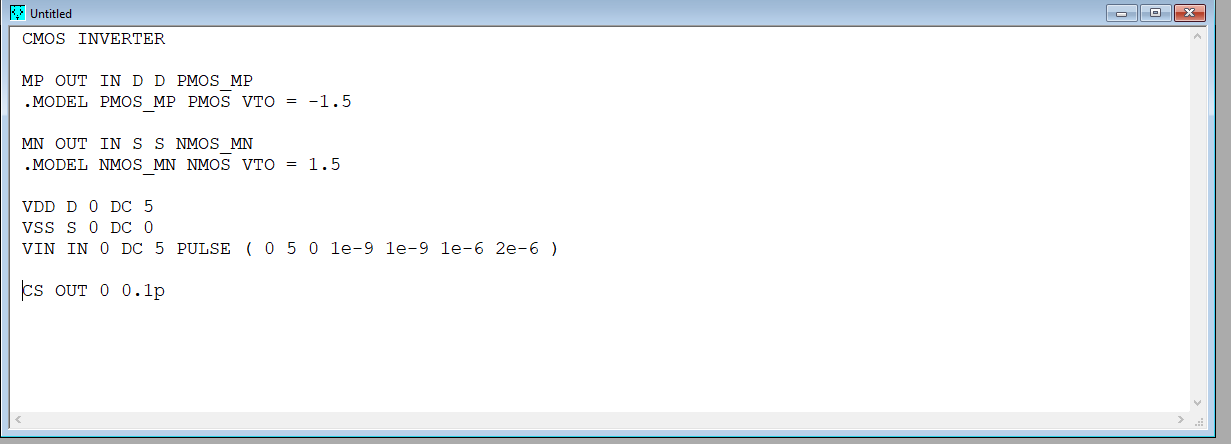
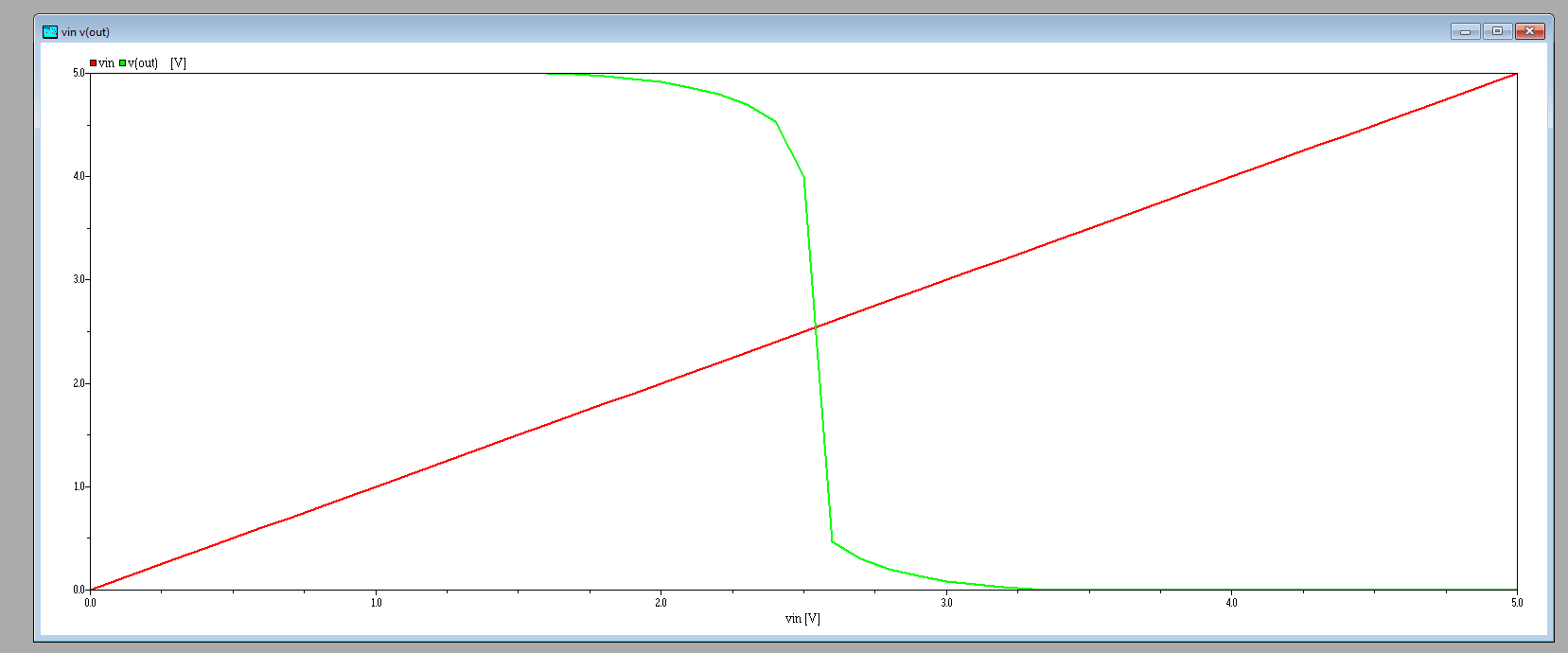
In today’s lab we implemeted a CMOS INVERTER using 2 MOS. In the upper part we use a PMOS gate and in the lower part of the circuit we have an NMOS circuit. PMOS is wired with NMOS and they form the INVERTER.If VIN is 0V then PMOS will conduct and the output will be 1. If VIN is 5V, then NMOS will conduct and PMOS will not so the output is 0.

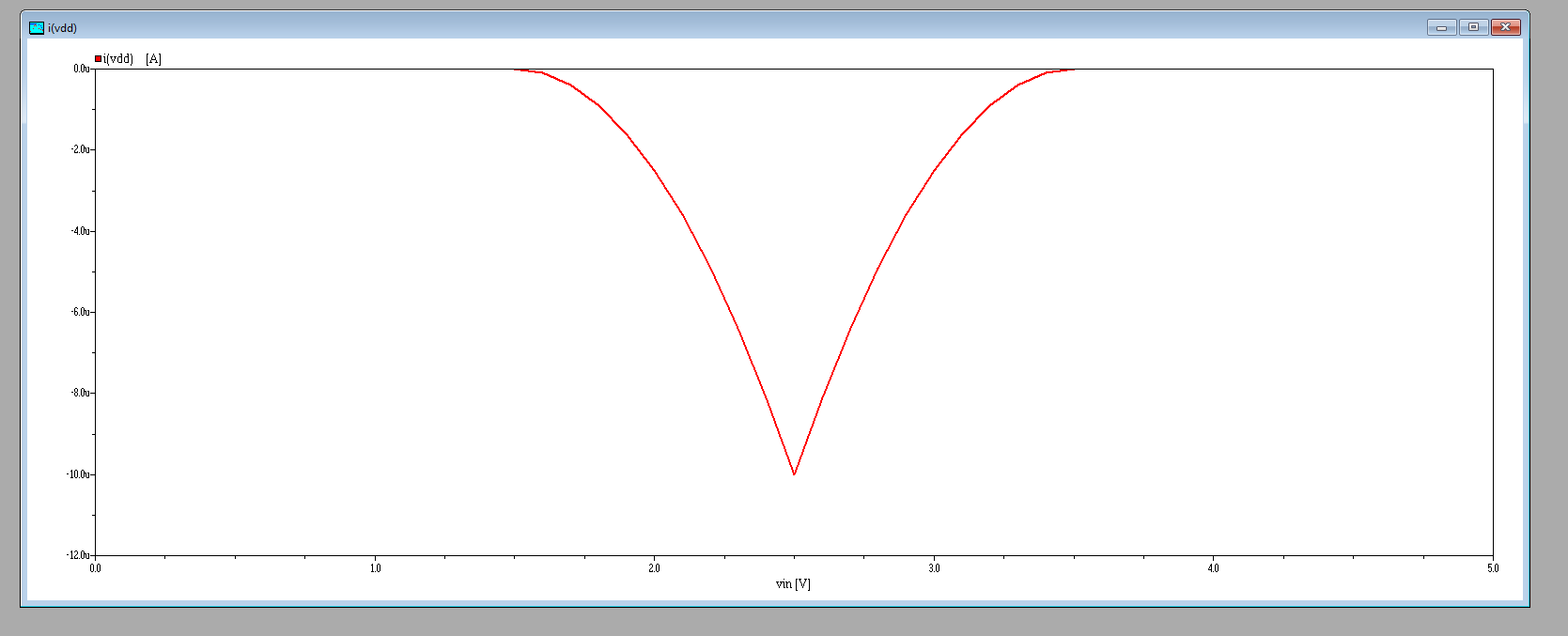
Code:



DC analysis :



I(VDD) DC :



We use the principle of the low-pass filter and we add an capacitor to smooth the transitions.

TR Analysis :

